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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,529	11/20/2003	Cheng-Liang (Andrew) Hou	58268.00325	6853

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EXAMINER	
CHU, WUTCHUNG	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,529	HOU, CHENG-LIANG (ANDREW)	
	Examiner	Art Unit	
	Wutchung Chu	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to application's amendment filed on 9/24/2007. Claims 1-17 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Rusu et al. (6137807).

Regarding claim 1, Rusu et al. disclose a dual bank queue memory and queue control system **(see column 1line 30-38)** comprising:

- receiving a packet **(see figure 5 box 305 cell input and column 2 line 28-29)**;
- determining an address of a free entry in a queue **(see figure 5 box 310 either bank 1 or 2 in use and 320 store and column 3 line 35-37 queue number)**;
- placing the determined address **(see column 3 lines 39-46 the multicast mask is a 46 bit attachment to a packet for indicating that the packet can be transmitted or routed anywhere)** in an entry of a prior-

determined address in the queue **(see column 3 lines 38-39 indicate start of a packet, end of packet, normal cell in a packet, and abort)** to form a linking list **(see figure 5 box 365 update link list for that queue and 51-53 each queue memory is assigned a set of linkage and mapping and at a processing components by the queue controller and column 4 line 55-57)**; and

- placing packet data of the packet in a free entry of a first data structure **(see figure 5 box 345 store cell in bank 1 and column 4 line 38-39)**,
- wherein there is one-to-one mapping between the queue and the first data structure **(see column 3 line 51-53 and column 4 line 66)**.

Regarding claim 2, Rusu et al. teaches the packet is unicast **(see figure 1B box 116a MAC input – it is inherent that in MAC organizationally Unique Identifier (OUI) field has a indication of whether it is unicast or multicast)**.

Regarding claim 3, Rusu et al. teaches the packet is multicast **(see column 3 line 39 multicast)** or broadcast, and further comprising:

- determining an address of a free entry in each queue associated with a destination in the packet **(see column5 line 20-24 and figure 6 box 460 begin transmission of output from chosen bank)**; and
- for each queue associated with a destination in the packet, placing the respective determined address in a respective entry of a prior-determined address in each respective queue **(see figure 6 box 420 and column 5 line 28-29)**.

Regarding claim 4, Rusu et al. teaches further comprising:

- determining a priority level for the received packet **(see column 6 line 29 and figure 6 box 425 find highest priority queue having first cell in the chosen bank (per link list))**; and
- wherein the placing the determined address places the determined address in an entry of a prior-determined address in the queue having the same priority **(see column 5 line 25-30, and it is inherent that address places the determined address in an entry of a prior-determined address in the queue having the same priority)**.

Regarding claim 5, Rusu et al. teaches the determining a priority level includes examining a quality of service field within the received packet **(see column 5 line 25-30 different priorities serves different services)**.

Regarding claim 6, Rusu et al. teaches further comprising updating free entry data to indicate that the determined address is in use **(see figure 5 box 360 update free list for the respective output queue)**.

Regarding claim 7, Rusu et al. teaches further comprising:

- placing a packet length of the packet in a free entry of a second data structure **(see column 3 lines 12-13 housekeeping and encapsulation (such as ensuring packet size and producing parity) is then perform, and col. 3 lines 51-56 each queue memory is assigned a asset of linkage and mapping and at a processing components by the queue**

controller, where components include a queue writer pointer, a queue reader pointer, a cell counter, a differential counter, and a maximum queue length. therefore the queue component maximum queue length is assigned to the memory); and

- wherein there is one-to-one mapping between the first data structure **(see column 3 line 51-53 and column 4 line 66 and figure 5 box 345 store cell in bank 1)** and the second data structure **(see figure 5 box 340 store cell in bank 2)**.

Regarding claim 8, Rusu et al. disclose a transmit queue system **(see column 2 line 18-19)** comprising:

- means for receiving a packet **(see figure 5 box 305 cell input and column 2 line 28-29)**;
- means for determining an address of a free entry in a queue **(see figure 5 box 310 either bank 1 or 2 in use and 320 store and column 3 line 35-37 queue number)**;
- means for placing the determined address **(see column 3 lines 39-46 the multicast mask is a 46 bit attachment to a packet for indicating that the packet can be transmitted or routed anywhere)** in an entry of a prior-determined address in the queue **(see column 3 lines 38-39 indicate start of a packet, end of packet, normal cell in a packet, and abort)** to form a linking list **(see figure 5 box 365 update link list for that queue and 51-53 each queue memory is assigned a set of linkage**

and mapping and at a processing components by the queue controller and column 4 line 55-57); and

- means for placing packet data of the packet in a free entry of a first data structure **(see figure 5 box 345 store cell in bank 1 and column 4 line 38-39)**, wherein there is one-to-one mapping between the queue and the first data structure **(see column 3 line 51-53 and column 4 line 66)**.

Note: the phrase "capable of" of "adapted to" recited in varies locations in claim 9 do not positively support claim limitations, therefore, the limitation after these phrases will not be considered as claimed limitations. However, the cited reference teaches the limitations (see rejection).

Regarding claims 9, Rusu et al. teaches transmit queue system, comprising:

- a first data structure capable of holding a plurality of packet data **(see figure 1A box 130 queue memory bank1)**;

- a queue capable of holding a linking list of addresses, the addresses having a one-to-one mapping **(see column 3 line 52 mapping)** with addresses in the first data structure **(see figure 2 box 102 link list management)**;

- a packet receiving engine capable of receiving a packet **(see figure 2 box 201 input arbiter)**;

- a free entry engine coupled to the packet receiving engine and capable of determining an address of a free entry in the queue **(see figure 4 box 146 free list RAM for Q1 and Q2)**;

- a transmit queue engine, coupled to the queue, the packet receiving engine and the free entry engine, capable of placing the determined address in an entry of a prior-determined address in the queue to form a linking list **(see figure 1 box 160output processor and figure 4 box 147 output port link list for q1 and q2, and figure 7 link lists)**; and

- a packet buffer engine **(see figure 2 box 104 queue buffer 1 controller)**, coupled to the first data structure, the packet receiving engine and the free entry engine, capable of placing packet data **(figure 2 ref 107)**of the packet in a free entry of the first data structure **(see figure 2 box 104 queue buffer 1 controller)**.

Regarding claims 10, Rusu et al. teaches a method, comprising:

- receiving an address in a queue **(see column 4 line 62-67)**;

- reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank and column 5 lines 31-34 the output arbitration subsystem coordinates the output demultiplexers to buffer and resegment the data from a chosen**

queue memory into an acceptable concatenated form for output, and it is inherent that the packet data to be read for it to be resegmented), the queue and the first data structure having one-to-one mapping **(see column 3 line 51-52)**;

- transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**;

- reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and

- using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Regarding claim 11, Rusu et al. teaches further comprising:

- reading a packet length of the packet in a free entry of a second data structure **(see column 3 lines 12-13 housekeeping and encapsulation (such as ensuring packet size and producing parity) is then perform, and col. 3 lines 51-56 each queue memory is assigned a asset of linkage and mapping and at a processing components by the queue controller, where components include a queue writer pointer, a queue reader pointer, a cell counter, a differential counter, and a**

maximum queue length. therefore the queue component maximum queue length is assigned to the memory); and

- wherein there is one-to-one mapping between the first data structure **(see column 3 line 51-53 and column 4 line 66 and figure 5 box 345 store cell in bank 1)** and the second data structure **(see figure 5 box 340 store cell in bank 2)**.

Regarding claim 12, Rusu et al. teaches the receiving receives an address **(see column 4 line 62-67)** for higher priority packet data before receiving an address for lower priority packet data **(see column 4 lines 25-28 the input processors to determine processing priorities, that is determined by the input processor with the highest priority, and column 5 lines 28-30 storing incoming data, utilizing the link list with the highest priority, therefore packet data are sorted with higher priority first and therefore the address of higher priority packet data is received before the lower ones)**.

Regarding claim 13, Rusu et al. teaches the packet data is multicast **(see column 3 line 39 multicast)** or broadcast and the transmitting transmits the packet data to a plurality of network nodes **(see column 3 lines 39-41 multicast mask is a 46 bit attachment to a packet for indicating that the packet can be transmitted or routed to anywhere)**.

Regarding claim 14, Rusu et al. teaches the packet is unicast **(see figure 1B box 116a MAC input – it is inherent that in MAC organizationally Unique Identifier (OUI) field has a indication of whether it is unicast or multicast)**.

Regarding claim 15, Rusu et al. teaches further comprising updating free entry data to indicate an address is free after the transmitting **(see figure 5 box 360 update free list for the respective output queue and figure 6 box 470 update link list and box 475 update free list)**.

Regarding claims 16, Rusu et al. teaches a transmit queue system **(see column 2 line 18-19)**, comprising:

- means for receiving an address in a queue **(see column 4 line 62-67)**;
- means for reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank and column 5 lines 31-34 the output arbitration subsystem coordinates the output demultiplexers to buffer and resegment the data from a chosen queue memory into an acceptable concatenated form for output, and it is inherent that the packet data to be read for it to be resegmented)**, the queue and the first data structure having one-to-one mapping **(see column 3 line 51-52)**;
- means for transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**;

- means for reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and

- means for using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Note: the phrase "capable of" of "adapted to" recited in claim 17 line 5 do not positively support claim limitations, therefore, the limitation after these phrases will not be considered as claimed limitations. However, the cited reference teaches the limitations (see rejection).

Regarding claims 17, Rusu et al. teaches a transmit queue system **(see column 2 line 18-19)**, comprising:

- a first data structure capable of holding a plurality of packet data **(see figure 1A box 130 queue memory bank1)**;

- a queue capable of holding a linking list of addresses, the addresses having a one-to-one mapping **(see column 3 line 52 mapping)** with addresses in the first data structure **(see figure 2 box 102 link list management)**;

- a packet transmit engine **(see figure 2 box 202 output arbiter)**, coupled to the first data structure and the queue, capable of

    - receiving an address in a queue **(see column 4 line 62-67)**;

- reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank)**;
- transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**;
- reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and
- using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Response to Arguments

3. Applicant's arguments filed 9/24/2007 have been fully considered but they are not persuasive.

4. **With regard to applicant's remark for claim 1 (page 12)**, applicant submit that the Rusu et al. fails to disclose or suggest that the queue number is placed in an entry or a prior-determined address in the queue to form a linking list, and "placing the determined address," and "entry of a prior-determined address in the queue to form a linking list."

Rusu et al. teaches multicast mask, a 46 bit attachment **(see col. 3 lines 32-46 corresponding placing the determined address)**, attach to a packet, and the control number which indicates start of a packet, end of packet, normal cell in a packet, and abort **(see col. 3 lines 32-46 corresponds to a prior-determined address in the queue)**. And Rusu et al teach link list which maintained by the queue controller organizes data stored in the available queue memory banks **(see col. 4 lines55-57)**, which applicant concurred.

The multicast mask attachment attach to the packet, where this packet is indicated by the queue controller of its position/address in the queue, which is either start of packet, or end of packet or as cited. And it is assigned to a set of linkage in the link list, which complies with all the limitations as claimed and the rejection maintains.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hsu et al. (US7088730); Aggarwal et al. (US2003/0081624)

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wutchung Chu whose telephone number is 571 270 1411. The examiner can normally be reached on Monday - Friday 1000 - 1500EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan D. Orgad can be reached on 571 272 7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WC/
Wutchung Chu

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